detecting an error position from the syndrome generated by said syndrome calculating means and by calculating an error value; an error detecting means for detecting an error, one sector at a time, in error-corrected data generated by said error correcting means; a bus control means for controlling data transfer between said buffer memory, said syndrome calculating means, said error correcting means, and said error detecting means; and a system control means for performing various processes for error correction in predetermined procedures a necessary number of times; wherein

said bus control means comprises:

a concurrent data transfer sub means for transferring data to be corrected from said buffer memory to said syndrome calculating means and to said error detecting means concurrently in code word units until said syndrome calculating means detects an error-containing code; and

an error-detecting data transfer sub means for, only when said syndrome calculating means has detected an error-containing code, after the error correction done by said error correcting means, transferring data in a sector containing_error-corrected data in and after the code word from which the error-containing code has been detected, from said buffer memory to said error detecting means for error detection,

said error detecting means comprises:

a parallel error detecting sub means for executing error detection for a code word transmitted from said buffer memory, in parallel with the syndrome calculation done by said syndrome calculating means; and

an error re-detecting sub means for, only when said syndrome

calculating means has detected an error-correcting code, executing error detection one more time for the error-corrected data.

4. The error correction device of claim 3 further comprising a DMA control means for controlling DMA transfer to said buffer memory, wherein

said system control means comprises:

a first DMA transfer sub means for providing said DMA control means with a first DMA transfer instruction indicating that data to be corrected should be transferred from said buffer memory to said syndrome calculating means and to said error detecting means at the start of an error correcting process; and

a second DMA transfer sub means for, after having been informed of completion of error correction by said error correcting means, only when said syndrome calculating means has detected an error-containing code, providing said DMA control means with a second DMA transfer instruction indicating that a sector containing the data from which said error-containing code has been detected should be transferred from said buffer memory to said error detecting means; and

said DMA control means comprises:

a transfer control sub means for making a request of said bus control means to perform DMA transfer in accordance with the first DMA transfer instruction and the second DMA transfer instruction transmitted by said system control means.

5. An error correction device comprising: a buffer memory for

storing at least one sector of data having a structure where each of N words of error correcting code comprises a data unit, an inner code parity unit, and one error detecting code; a syndrome calculating means for generating syndrome for data read from said buffer memory; an error correcting means for correcting error-containing data in said buffer memory by detecting an error position from the syndrome generated by said syndrome calculating means and by calculating an error value; an error detecting means for detecting an error, one sector at a time, in error-corrected data generated by said error correcting means; a storing means for storing mid-term results, in code word units, of an error detecting process in said error detecting means; a bus control means for controlling data transfer between said buffer memory, said syndrome calculating means, said error correcting means, and said error detecting means; and a system control means for performing various processes for error correction in predetermined procedures a necessary number of times, wherein

said bus control means comprises:

a first transfer sub means for executing a first transfer where data to be corrected are transferred in code word units from said buffer memory concurrently to said syndrome calculating means and to said error detecting means until said syndrome calculating means detects an error-containing code, and for suspending the first transfer when said syndrome calculating means has detected an error-containing code; and

a second transfer sub means for executing a second transfer where a code word from which an error has been detected and corrected is transferred from said buffer memory to said error detecting means after